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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,217	06/24/2003	Eric E. Edwards	X-1330 US	4304

24309 7590 02/09/2005

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EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,217	EDWARDS, ERIC E.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-7,9-13 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13,19 and 20* is/are allowed.

6)☒ Claim(s) *2-7, 9-12, and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment submitted on Nov 8, 2004 was reviewed and considered with the following results:

Amended paragraphs 0028 and 0031 overcame the objections to the disclosure that were described in the previous Office Action. Therefore, those objections have been withdrawn.

Amended claims 12-13 overcame their objection as being dependent upon a rejected base claim, and those objections have been withdrawn. However, after reconsidering the first/second capacitor limitations of claim 12, it was determined those features are not novel, patentable features, and the indication of allowable subject matter, with respect to claim 12, has now been withdrawn. Therefore, claim 12, and its dependent claims, are rejected as described later under the appropriate section. Due to these new rejections, this action is NON-FINAL.

The cancellation of claims 1, 8, and 14-18 rendered their respective rejections moot.

The amended claims overcame the previous Office Action's prior art rejections of: 1) claims 2-3, and 10-11 under 35 U.S.C. 102(b) with respect to Frisch et al.; 2) claims 2-4, and 10-11 under 35 U.S.C. 102(b) with respect to Guritz; 3) claims 2-3, and 6 under 35 U.S.C. 102(b) with respect to Chevallier et al.; 4) claims 4-7, and 9 under 35 U.S.C. 103(a) with respect to Frisch et al.; and 5) claims 5-7, and 9 under 35 U.S.C. 103(a) with respect to Guritz. All of those original prior art rejections have now been withdrawn because none of these references clearly shows or discloses the plurality of first diode connected transistors, the first resistor, and their respective "between the first input" related limitation now recited within amended claim 4; or the first/second capacitor limitations recited within claim 12, upon which claims 9-11 now depend.

However, new and/or modified rejections are described later under the appropriate sections, and associated comments are described under the Response to Arguments.

Claim Objections

Claims 2, 3, 5, and 6 are objected to because of the following informalities: Since claim 4 recites the plurality of first diode connected transistors are connected in series, and this series is connected to the first input, it is understood this plurality will have one diode connected transistor coupled to the first input. Therefore, it is suggested "the at least one diode connected transistor" on lines 1-2 of claim 2 be changed to --the one first diode connected transistor-- to clearly relate the transistor to the "first" transistors (e.g. different from the "at least one second diode connected transistor"), and also to minimize the possibility that the phrase "at least one...transistor" could imply more than one of the first and/or second transistors can be coupled to the first input. For consistent labeling, it is suggested "one diode" on line 2 of claim 3 be changed to --one second diode--. Claim 5, line 2 "are" should be --is-- to correspond to its single subject "plurality", and it is suggested "ground" on line 3 be preceded by --the-- since that potential was already identified in independent claim 4. Claim 6, line 5 "ground" should be followed by --potential-- for consistent labeling throughout the claims. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2-7, and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the

applicant regards as the invention. Claim 4, line 5 "a plurality of first diode connected transistors connected in series" is confusing. For example, are the transistors connected in series, or is more than one plurality implied, wherein those pluralities are connected in series? Clarification is requested with respect to what "at least one resistor divider coupled between the second input and ground potential" means on lines 8-9 of claim 4. For example, is the entire resistor divider, or only a portion of it (e.g. one resistor), actually coupled between the second input and the ground potential? It is not clear what is meant by "the hysteresis circuit configured to protect the power up reset circuit from glitches" as recited on lines 3-4 of claim 6. For example, does the hysteresis circuit minimize inadvertent type reset signals with respect to glitches, or actually protect the overall power up reset circuit from possible structural or functional type damage caused by glitches (e.g. ESD events)? It is not understood how the first diode connected transistor of claim 13 can be connected directly to ground as recited within claim 21, when it is already connected to the third resistor (e.g. see the last line of claim 13). For example, the applicant's own Figs. 9 and 10 both show first diode connected transistor T6 coupled to third resistor R2. However, even if (enable) transistor T3 is replaced by a direct connection to ground, T6 is still coupled through either third resistor R2 and/or transistor T7 of the hysteresis circuit. Therefore, claim 21's direct connection to ground needs clarification.

Claim 7 recites the limitation "the hysteresis circuit" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

In so far as being understood, claims 2-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Tabata, a reference not previously cited. Fig. 6 shows a power up reset circuit comprising comparator B having first/second inputs a/b, and output c; plurality of series connected first diode connected transistors 1-2 between first input a and power supply voltage VDD; first resistor 3 connected between first input a and ground potential; section 9 of resistor divider C is coupled between second input b and the ground potential; and a reset signal will be generated at output c when the voltages at the inputs are approximately the same (e.g. see column 7, lines 20-45), thus anticipating claim 4. The voltage at first input a will be maintained at a one or more threshold voltage difference from power supply voltage because of the threshold drops of transistors 1-2 (e.g. see column 5, lines 34-67), anticipating claim 2. One of ordinary skill in the art would also understand the resistor divider coupled to second input b will try to maintain a one or more threshold voltage difference from the ground potential. This anticipates claim 3.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frisch et al. (Frisch), a reference cited in the previous Office Action. Fig. 4

shows power up reset circuit 20 comprising comparator 38 with first/second inputs 29/36 and output 41; first diode connected transistor 24 connected between first input 29 and power supply voltage Vdd; first resistor 26 connected between first input 29 and ground potential Vss; second diode connected transistor 34 coupled between second input 36 and ground potential Vss, wherein a reset signal at output 41 (corresponding to signal POR) is generated when the voltages at first/second inputs 29/36 are approximately the same (e.g. see the lower right graph showing Vdd, 29, 36, and 46). However, the reference does not show a plurality of first diode connected transistors 24. It would have been obvious to one of ordinary skill in the art to replace single transistor 24 with a plurality of series connected transistors that are each diode connected, thus rendering claim 4 obvious. The plurality of first transistors would provide a means for delaying the reset signal, thus corresponding to when a higher level of power supply voltage Vdd is reached. For example, the voltage at first input 29 would not begin to increase from ground until the power supply voltage has reached at least the combine threshold voltage of all of the series connected transistors 24. Using the upper graph of Fig. 4 as a reference, when transistor 24 is replaced by at least two diode connected transistors, which are coupled in series, line 29 would shift to the right. The diode connected first transistors would try to maintain at least one threshold voltage difference from power supply voltage Vdd, rendering claim 2 obvious. Second diode connected transistor 34 tries to maintain at least one threshold voltage difference from ground potential Vss, and claim 3 is rendered obvious. It also would have been obvious to one of ordinary skill in the art to replace single second transistor 34 with at least two second diode connected transistors that are coupled in series, thus rendering claim 5 obvious. This would also provide a means for delaying the reset signal. For example, the voltage at second input 36 would

not begin to stabilize (e.g. level off) until power supply voltage Vdd has reached at least the combine threshold voltage of all of the series connected transistors 34. Using the lower left graph of Fig. 4 as a reference, when transistor 34 is replaced by at least two diode connected transistors, that are coupled in series, line 36 would start to divert away from Vdd at a higher voltage, and at a later time.

In so far as being understood, claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tabata as applied to claim 4 above, and further in view of Degoirat et al. (Degoirat), another reference not cited in a previous action. As described above, Tabata shows a circuit comprising the recited limitations of claim 4. However, the reference does not clearly show or disclose a hysteresis circuit. Degoirat shows and discloses various hysteresis type circuits with respect to a voltage divider that provides a voltage to one input of a comparator of a power up reset circuit. For example, Fig. 4 shows an unlabeled switch coupled in parallel to resistor R2 of resistor divider R1-R3. This configuration allows the switching threshold of the comparator to be changed to avoid instabilities (e.g. see column 4, lines 10-26). Therefore, it would have been obvious to one of ordinary skill in the art to replace Tabata's voltage divider C with the voltage divider R1-R3 and hysteresis circuit (e.g. the unlabeled switch) of Degoirat. The hysteresis circuit will help avoid instabilities with respect to the power supply voltage VDD being close to the switching threshold. For example, near the switching threshold of the comparator, noise or fluctuations on the power supply voltage or ground potential could inadvertently trigger the comparator if no hysteresis circuit is used. Therefore, Degoirat's hysteresis circuit/resistor divider combination will effectively protect the power up reset circuit from glitches, rendering claim 6 obvious. When the switch across resistor R2 is closed, the

corresponding voltage Vref1 (applied to second input b) is lowered (e.g. see column 4, lines 14-25), causing the switching threshold to be changed. Therefore, the hysteresis circuit effectively lowers the power supply voltage to the comparator of the power up reset circuit, thus changing the reset signal and rendering claim 7 obvious.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guritz, a reference cited in the previous Office Action. Fig. 9 shows power up reset circuit 10 comprising comparator 14 having first/second inputs V1/V2 and output 16. The first/second inputs are coupled to circuit blocks 18/20 respectively, which can correspond to the various networks shown in Figs. 3a, 4a, 4b, 5a, and 5b (e.g. see column 4, lines 37-40), wherein the 18/20 combination provides signals V1/V2 that cross (e.g. see Figs. 6-8). Since Guritz discloses that the LOAD (e.g. see Figs. 4a, 4b, 5a, and 5b) can be a resistor (e.g. see column 3, lines 35-36), the following descriptions will assume a resistor is the LOAD. However, the reference does not clearly show or disclose a plurality of diode connected transistors connected in series between an input and either a power supply voltage or ground potential. It would have been obvious to one of ordinary skill in the art to use a variation of Fig 4a as one of blocks 18/20, and either the resistor divider of Fig. 3a, or a variation of Fig. 5b for the other one of blocks 18/20. One of ordinary skill in the art would realize that Fig. 4a could comprise a plurality of

series coupled diode connected transistors T1 coupled between VDD and VR, with VR connected to the first input. Therefore, there would be more than one first diode connected transistor coupled in series between the first input and power supply voltage VDD. With either Fig. 3a or Fig. 5b coupled to the second input, there would be at least one diode connected transistor (i.e. T2 of Fig. 5b) or at least one resistor (i.e. R2 of Fig. 3a) coupled between the second input and the ground potential. Since the reset signal would be generated at output 16 once the two input voltages are approximately the same (e.g. the voltages cross as shown in Figs. 6 and 8), claim 4 is rendered obvious. The plurality of diode connected transistors would provide a means for delaying when the reset signal is generated, because the increase of VR from ground (e.g. see Fig. 4) would not occur until power supply voltage VDD has reached the switching threshold of the plurality of series transistors. Therefore, by changing the number of diode connected transistors T1 coupled between VDD and VR, changes when the reset signal will be switched, and one of ordinary skill in the art would understand this switching time depends on the desired switching delay and/or minimum power supply voltage. The diode connected transistors coupled to the first input would try to maintain at least a one threshold difference from the power supply voltage at the first node, and claim 2 is rendered obvious. Similarly, the one diode connected transistor (of Fig. 5b) or the resistor divider (of Fig. 3a) would try to maintain at least one threshold voltage difference from ground, rendering obvious claim 3. Using a variation of Fig 5b, it would have been obvious to one of ordinary skill in the art to replace the single second diode T2 with a plurality of series connected second diode connected transistors between the second input and ground. This renders claim 5 obvious. With this type of configuration, the increase of VR would begin to at least stabilize (or level off) once

power supply voltage VDD reaches the threshold value of the plurality of transistors. The configuration of the circuit coupled to the second input can be varied as another means to determine when the reset signal will actually be generated, because the reset signal requires both the first/second input potentials of the comparator to be approximately equal before the reset signal is generated (e.g. changed).

Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guritz, in view of Furuchi, another reference not cited in the previous Office Action. As previously described with respect to claim 4 above, Fig 9 of Guritz shows comparator 10 with its first/second inputs coupled to circuit blocks 18/20, respectively. Since Guritz discloses the various circuit networks shown in Figs. 4a, 4b, 5a, and 5b can be used to provide the desired characteristic curves (e.g. see column 4, lines 35-40), one of ordinary skill in the art would understand that the combination of Figs. 4a/5b, or of Figs. 4b/5a could be used for blocks 18/20. In each combination, power supply VDD will be coupled directly to a first resistor (see the LOAD shown in Figs. 4b and 5b) with the other end of the resistor being connected directly to input VR; a first diode connected transistor (see T3 of Fig. 4b or T2 of Fig. 5b) connected directly to ground, and it other end connected to input VR; second diode connected transistor (see T1 of Fig. 4a or T4 of Fig. 5a) coupled directly to power supply VDD, and its other end connected to input VR; and second resistor (see the LOAD shown in Figs. 4a and 5a) connected directly to ground, with its other end connected to input VR. However, the reference does not show or disclose reset signal 16 (produced by comparator 14) as being connected to first/second capacitors that are coupled in series between the power supply and ground; or that the IC comprises a Field Programmable Gate Array (FPGA). Column 1, lines 23-38 of Guritz discloses

the use of delay circuitry might possibly be used to minimize premature operation. Furuchi shows and discloses the use of first/second capacitors C1/C2 coupled between power supply Vdd and ground as a delay type means for resisting noise on the power supply or ground (e.g. see the abstract). In Fig. 3, these two capacitors are coupled to the digital/logical output of inverter 101. Therefore, it would have been obvious to one of ordinary skill in the art to apply the teaching of Furuchi to the circuit of Guritz. In this case, it would have been obvious to couple first capacitor C1 between output node 16 (of Guritz) and power supply VDD, and couple second capacitor C2 between output node 16 and ground, thus rendering claims 11 and 12 obvious. The use of first/second capacitors C1/C2 with Guritz's circuit will help maintain the reset signal at output node 16, even if there is a temporary fluctuation (e.g. noise or a glitch) with respect to either the power supply or ground. The capacitors would also provide a means for adjusting the overall delay of the circuit to ensure the reset signal will not be provided until the power supply voltage has reached its minimum value, after at least a minimum amount of time. One of ordinary skill in the art would understand the output of comparator 14 would be provided as first (or high) and second (or low) logic level output states due to inverter 30, thus rendering claim 10 obvious. Column 5, lines 1-6 of Guritz discloses that the reset signal can be used to clear registers, reset timing, etc. Therefore, it would have been obvious to one of ordinary skill in the art to use the IC's power up reset circuit with a FPGA, rendering claim 9 obvious. This can be considered intended use, as it is well known to one of ordinary skill in the art that the operation of a FPGA should not proceed until the power supply has reached at least a minimum, predetermined level. Also, the reset signal can be used to ensure the stored data within a FPGA has been reset, thus

avoiding possible indefinite values when the FPGA is used during normal operations after a power up type sequence.

Claims 9-12 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Frisch et al. (Frisch), in view of Furuchi, for the same reasoning as described above with respect to the rejections of claims 9-12 using the Guritz/Furuchi references. Therefore, it is not considered necessary to basically repeat all the details again other than Furuchi's first/second capacitors C1/C2 could be coupled to output node 41 of Frisch to minimize incorrect switching of the reset signal, rendering claims 9-12 obvious.

Allowable Subject Matter

Claims 13, and 19-20 are allowed. There is no motivation to modify or combine any prior art reference(s) to ensure the circuit includes a hysteresis circuit, with a feedback transistor and third resistor, as recited within claim 13, upon which claims 19-20 depend.

Response to Arguments

The applicant's arguments filed Nov 8, 2004 have been fully considered but they are not persuasive. The argument that Guritz's plurality of diode connected transistors are not connected between the first input node and the power supply point is only correct for claim 4 as now amended, and therefore the examiner agrees that "Claim 4 is not anticipated by Guritz" (e.g. see page 8 of the amendment). This is because not every element of the amended claim is clearly shown or disclosed with respect to a rejection made under 35 U.S.C. 102. However, original claim 4 only recited the first plurality of diode connected transistors was coupled in series, and the plurality was also coupled to the first input. Guritz's transistors T5 and T6, shown in Fig. 4C, are clearly coupled in series, and their common connection VR would be coupled to the first

input. As for the 35 U.S.C. 102 related rejection, claim 4 was clearly rejected under 35 U.S.C. 103 as described on the previous Office Action's pages 5-6. Therefore, all of the previous Office Action's rejections were proper with respect to the limitations that were originally recited.

Related to the above arguments/comments, the applicant's arguments with respect to claim 4 are moot in view of the new ground(s) of rejection. The amended claim now clearly recites the plurality of first diode connected transistors are connected between the first input and a power supply voltage, wherein the amended claim also now includes a first resistor connected between the first input and ground. Therefore, the original rejection of claim 4 has been modified to account for these amended changes.

The applicant's arguments, with respect to a plurality of diode connected transistors, have been fully considered but they are also not persuasive. It appears that the applicant does not believe one of ordinary skill in the art would know that the number of series coupled diode connected transistors can be changed to change the overall threshold (or voltage) drop across the transistors. It also appears the applicant requires every prior art reference to clearly show and disclose each single detail; even if it would be well known to one of ordinary skill in the art. To support the examiner's obvious type rejections with respect to a plurality of diode connected transistors, several other prior art references are cited on the accompanying PTO-892. These references are described later.

Therefore, the prior art rejections described in this action, and in the previous Office Action, are deemed proper with respect to the knowledge of one of ordinary skill in the art, and to the prior art references cited in this action, or in the previous Office Action.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant for at least sections of the claimed limitations. The references of Woods and Payne et al. are examples that both clearly show and disclose power up reset type circuits comprising at least two diode connected transistors (or diodes) connected in series with at least one resistor, wherein those series coupled components are coupled between a power supply voltage and ground. For example, see Woods (Fig. 1: 110,120) and Payne et al. (Fig. 3: 305,312). Column 2, lines 61-64 of Woods states that "any number of dual diodes 112,..., or other solid state devices" can be used depending on the desired voltage drop. Payne et al. discloses "it is obvious to a person of ordinary skill in the art that many diodes can be stacked in series" (i.e. see column 4, lines 64-67). Fig. 3 of Kitade closely corresponds to the applicant's own Fig. 5. For example, diodes 121n-123n, resister 121r, comparator 130, resistor 111r, and diodes 111n-113n of Kitade correspond to 324-1-324-M1, 326, comparator, 320, and 322-1-322-N1, respectively. The basic difference is Kitade's output includes complementary signals A,B, wherein the applicant's output is shown as single signal PUR. Therefore, since these references provide support showing and/or disclosing that the number of diode connected transistors (that are coupled in series) can be changed, and/or that two different diode connected/resistor type voltage dividers can provide the two input signals to a comparator, the references should be carefully reviewed and considered with respect to the basic limitations claimed.

Note: The reference of Maccarrone et al., cited in the previous Office Action, shows the output of comparator 2 (of power up reset circuit 1) coupled to capacitor C in Fig. 2. Although that figure shows the capacitor coupled between the output node A and power supply vdd, the

reference of Furuchi (described above in the present action), discloses a single capacitor can be replaced by a functionally equivalent plurality of capacitors coupled between the power supply and ground to help prevent malfunctions resulting from noise on the power supply and/or on ground (e.g. see column 4, lines 8-18). Applying this teaching to capacitor C of Maccarrone, that capacitor could be replaced with one capacitor coupled between output node A and power supply vdd, and another capacitor could be coupled between output node A and ground. Therefore, the output of a power up reset circuit would be coupled to a common node of first/second capacitors, thus the first/second capacitor limitations of claim 12 are no longer considered allowable material.

For the record, this examiner, as one of ordinary skill in the art, knows that a comparator within a power up reset circuit can have its inputs coupled to circuits that each comprise at least one diode connected transistor, and at least one resistor, wherein each set of diode connected transistor(s) and resistor(s) is coupled in series between a power supply voltage and ground. This knowledge is clearly supported by at least four references cited within this action, or the previous Office Action (e.g. see Frisch et al. (e.g. Fig. 4); Guritz (Fig. 9 with respect to Figs. 4a-4c, 5a, and 5b); Kitade (Fig. 3); and Kwon (Figs. 5, and 7-8)). Therefore, these basic limitations, including the use of a plurality of diode connected transistors, are not deemed to be novel, patentable features of the present invention.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

4 February 2005

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